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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,216	07/22/2003	Terrance J. Dishongh	42P13858C	8364

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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,216	DISHONGH ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on 24 January 2005. These drawings are acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 31-44, 45, and 47-55 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,555,208 (hereafter Takada).

Takada discloses, referring to figure 4, a printed circuit board (PCB) comprising: a first signal routing layer (201) formed on a first surface of the PCB; an electrically conductive layer (202), at least one padless via (203) extending from the first signal routing layer to the electrically conductive layer, the at least one padless via in electrical contact with the electrically conductive layer (see col. 14, lines 10-20); and a layer of solder mask material (261) formed over the first signal routing layer, the layer of solder mask material having at least one opening (263) to expose the at least one padless via [claim 31], wherein the electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on

the second signal routing layer (see col. 14, lines 10-20), further comprising a via plug (205) formed within the padless via [claim 33], wherein the via plug is formed of an electrically conductive material (col. 14, lines 10-20) [claim 34], further comprising a component (308, figure 3) attached to the PCB with a solder interconnection between a contact pad on a bottom surface of the component and the at least one padless via [claim 35].

Similarly, Takada discloses, referring to figure 2, a printed circuit board (PCB) comprising: a first signal routing layer (201) formed on a first surface of the PCB; at least one electrically conductive layer (202), and an array of interconnections formed on the first surface of the PCB, the array of interconnections including at least one padless via (203) extending from the first signal routing layer to the at least one electrically conductive layer, wherein the padless via is in electrical contact with the at least electrically conductive layer (col. 14, lines 10-20) [claims 36, 47], wherein the at least one electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer (col. 14, lines 10-20) [claims 37, 48], further comprising an electrically conductive via plug (205) formed within the at least one padless via [claims 38, 51], wherein the array of interconnections further comprises at least one contact pad (301, figure 8) electrically coupled with a conductive trace on the first signal routing layer, wherein the at least one contact pad has a diameter less than 18 mils (col. 16, lines 15-20), wherein the at least one padless via has a diameter of 12 mils or less (col. 14, lines 20-30).

Furthermore, Takada discloses, referring to figure 2, a system comprising: a printed circuit board (PCB) including a first signal routing layer (201) formed on a first surface of the PCB, at least one electrically conductive layer, and an array of interconnections formed on the first surface of the PCB, wherein the array of interconnections includes at least one padless via (203) extending from the first signal routing layer to the at least one electrically conductive layer, the at least one padless via electrically connected to the at least one electrically conductive layer (col. 14, lines 10-20); and a component attached to the PCB by a plurality of solder ball interconnections between the array of interconnections formed on the first surface of the PCB and a corresponding array of contact pads disposed on a bottom surface of the electronic component (col. 16, lines 1-35) [claim 41], wherein the at least one electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer (col. 14, lines 10-20) [claims 42, 48], further comprising at least two conductive traces on the first signal routing layer routed between the at least one padless via and an adjacent interconnection (fig. 3) [claims 43, 50], wherein the at least one padless via has a diameter of 12 mils or less (col. 14, lines 20-30), wherein forming a via plug within the at least one padless via comprises overplating the at least one padless via to form a via plug of plating material (see col. 14, line 60 – col. 15, line 10) [claim 52].

Moreover, Takada discloses, a method of attaching a component to a printed circuit board (PCB) comprising: aligning solder balls (310) attached to an array of contact pads on a bottom surface of the component (308) with a corresponding array of

interconnections formed on a first surface of the PCB, the array of interconnections comprising at least one padless via (203) extending from a first signal routing layer (201) on the first surface of the PCB to an electrically conductive layer, wherein the at least one padless via is in electrical contact with the electrically conductive layer; and reflowing the solder balls to electrically connect the array of contact pads to the corresponding array of interconnections [claim 54], wherein the electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer (col. 14, lines 10-20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takada.

Takada discloses the claimed invention as described above except Takada does not specifically state that a width of the at least two conductive traces is approximately 3 mils. Instead, Takada generically states that the width can be varied (see col. 15, lines 25-35). Therefore it would have been obvious, to one having ordinary skill in the art, at the time of invention, to make the width 3 mils. The motivation for doing so would have been to provide a conductor of width sufficient to handle the required signal propagation, yet small enough to avoid wasting board space. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Claims 46, 56, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takada in view of US 2003/0001287 A1 (hereafter Sathe).

Takada discloses the claimed invention as described above except Takada does not specifically state that the PCB is a motherboard and the component is a processor

[claim 46] nor that the component is an electronic component housed in a ball grid array (BGA) package having a BGA pitch of 0.8 mm or less [claim 56] nor wherein the component is a land grid array (LGA) socket [claim 57]. Takada simply states that the component is a partner member. It is well known in the art, as evidenced by the disclosure of Sathe, that a PCB, such as the one disclosed by Takada could be considered a mother board, (see Sathe [0002]) and that additionally processors are attached to said boards (Sathe [0002]-[0004]). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to comprise the board and component in Takada of a motherboard and a processor respectively. the motivation for doing so would have been to form an electronic assembly for an electronic system such as a computer (Sathe [0002]).

Similarly, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to comprise the component of a well-known BGA package (Sathe [0024]) or LGA package (Sathe [0079]). Moreover, although the modified invention of Takada does not specifically state that the BGA pitch is 0.8mm or less such a modification would have be trivial for the ordinarily skilled artisan. The motivation for doing so would have been to choose a pitch wide enough to avoid short circuiting yet small enough to reduce the footprint of the device, thus freeing premium board space for additional wiring. Additionally, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Response to Arguments

Applicant's arguments filed 24 January 2005 have been fully considered but they are not persuasive. Applicants' solely argue that the claimed invention distinguishes over the prior art of record because "Takada fails to teach a padless via". Applicants assert that Takada only discloses a "via-in-pad" structure. However, this is at best a limited reading of the disclosure of Takada. Takada specifically states, "the above conductor pattern is all conductive patterns which are able to be formed on the surface of the insulating substrate such as a wiring circuit, a pad, a terminal, a land, etc." It would be readily understood to the ordinarily skilled artisan that the "wiring circuit" discloses here is fundamentally different from the "pad" Applicants insist **must** be present in the invention of Takada. This conductor pattern being a wiring circuit would indeed be a "padless". Thus Applicants' traversal of the instant rejection on this ground is deemed unsuccessful.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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